UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,011	11/26/2003	Christoph Heer	2002 P 10624 US	7561

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EXAMINER
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ART UNIT	PAPER NUMBER
2129	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/724,011	HEER, CHRISTOPH
	Examiner	**Art Unit**	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>26 November 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-14</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-14</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>26 November 2003</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>3/9/2004</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

Detailed Action

1.   Claims 1-14 are pending in this application.

Drawings

2.   Per claim 1, the CLB control logic is suppose to have 4 inputs and a single

output. In the figure there are 6 inputs.

This objection must be corrected.

Specification Objection

3.   Abstract states that the invention 'realizes' an 'if-then-else' branch. This is

ambiguous such that does it mean it can identify a 'if-then-else' statement or does it

solve a 'if-then-else' statement. If it identifies an 'if-then-else' statement it would need 3

comparisons for 'if', 'then' and 'else' in the look up table. If it were to solve the 'if-then-

else' statement it would need only one comparison because a 'if-then-else' only has one

comparison.

Claim Objections

4.   Claim 1 states there are 4 inputs and 1 output for the CLB control logic circuit.

The lone figure shows 5 inputs, the fifth input being a clock pulse.

This objection must be corrected.

35 USC § 101

5.   35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine,
manufacture, or composition of matter, or any new and useful improvement
thereof, may obtain a patent therefor, subject to the conditions and requirements
of this title.

Claims 1-14 are rejected under 35 U.S.C. 101 for nonstatutory subject matter. If

the "acts" of a claimed process manipulate only numbers, abstract concepts or ideas

representing any of the foregoing, the acts are not being applied to appropriate subject

matter. Schrader, 22 F.3d at 294-95, 30 USPQ2d at 1458-59. See MPEP 2100-12.

Claims 3, 6, 9, and 11 are rejected under 35 U.S.C. 101 for lack of functional

description. Connection between modules with no explanation serves no function.

Claim Rejections - 35 USC § 112

6.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The phrase 'input control node" is not defined in the specification.

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Mano, and further in view of Barstow, and further in view of Hellestrand, and further in view of Miller, and further in view of Udagawa, and

further in view of Nataraj, and further in view of Nomura (U. S. Patent Publication

20020152060, referred to as **Tseng**; 'Logic and Computer Design Fundamentals,

2nd Edition Updated', referred to as **Mano**; U. S. Patent 4827404, referred to as

Barstow; U. S. Patent Publication 20020019969, referred to as **Hellestrand**;

U. S. Patent 6181164, referred to as **Miller**; U. S. Patent 6388767, referred to as

Udagawa; U. S. Patent Publication 20020161969, referred to as **Nataraj**; U. S.

Patent 6317362, referred to as **Nomura**).

Claim 1.

Tseng teaches an input data node for carrying input data (**Tseng**, ¶[0523]).

Tseng does not teach a CLB control logic circuit having a first input, a second

input, a third input, a fourth input and an output. Mano teaches teach a CLB control

logic circuit having a first input, a second input, a third input, a fourth input and an output

(**Mano**, Page 351, figure 7-5 (The components of the OR gate, the MUX and the load

comprise the control logic circuit); EN The CLB control logic can be anything. This figure

illustrates the four inputs being K1, K2, output of R2 and output for R1. There is a fifth

input for the clock (See claim specification) The output is Q_0-Q_3 from R0.). It would have

been obvious to a person having ordinary skill in the art at the time of applicant's

invention to modify teachings of Tseng by having a control unit that uses current input to

dictate the operations of the CLB as taught by Mano to have a CLB control logic circuit

having a first input, a second input, a third input, a fourth input and an output.

For the purpose of the CLB to operate with current information.

Tseng and Mano do not teach at least one look-up table in which a switching

function of at least one conditional branch is implemented with content addressability,

wherein the at least one look-up table generates an "if then else" branch that realizes a

comparison of the input data with comparison data previously stored in the at least one

look-up table, and wherein a result output of the at least one look-up table is provided to

a third input of the CLB control logic. Barstow teaches at least one look-up table in

which a switching function of at least one conditional branch is implemented with

content addressability, wherein the at least one look-up table generates an "if then else"

branch that realizes a comparison of the input data with comparison data previously

stored in the at least one look-up table, and wherein a result output of the at least one

look-up table is provided to a third input of the CLB control logic (**Barstow**, C12:36

through C13:2 and C14:65 through C15:17; EN In C12:36 through C13:2 Barstow

illustrates the steps taken when going through the 'if' , 'then' and 'else' conditions. In

order to make the changes between these steps is called a switch which Barstow

illustrates in C14:65 through C15:17.). It would have been obvious to a person having

ordinary skill in the art at the time of applicant's invention to modify combined teachings

of Tseng and Mano by giving the details on how a look-up table work in finding a if-then-

else statement as taught by Barstow to have at least one look-up table in which a

switching function of at least one conditional branch is implemented with content

addressability, wherein the at least one look-up table generates an "if then else" branch

that realizes a comparison of the input data with comparison data previously stored in

the at least one look-up table, and wherein a result output of the at least one look-up table is provided to a third input of the CLB control logic.

For the purpose of having the ability to identify a if-then-else statement.

Tseng teaches an input data bus coupled between the input data node and a bus input of the at least one look-up table, wherein the first input of the CLB control logic circuit is coupled to the input data node via the input data bus(**Tseng**, ¶[0242]).

Tseng, Mano and Barstow do not teach at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to a fourth input of the CLB control logic. Hellestrand teaches at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to a fourth input of the CLB control logic (**Hellestrand**, ¶[0310], ¶[0311] and figure 16; EN In figure 16, item 1609 is a multiplexer and 'asynch event control of Hellestrand is equivalent to 'logic circuit' of applicant.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to combined teachings of Tseng, Mano and Barstow by having the control logic operate with current input data as taught by Hellestrand to have at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to a fourth input of the CLB control logic.

For the purpose of operating with current inputted data results in improved results.

A control input node coupled via a control bus to the second input of the CLB control logic (See Claim Rejections - 35 USC § 112).

Tseng, Mano, Barstow and Hellstrand do not teach at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer. Miller teaches at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer (**Miller**, figure 4 and C5:47-51). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Tseng, Mano, Barstow and Hellstrand by illustrating the connections between the modules as taught by Mlller to have at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

For the purpose of using the inputted data and comparing it with what is stored in the registers with the results of this look up table being sent to a multiplexer for a frther decision to be made then.

Claim 2.

Tseng does not teach a register which stores the comparison data; and a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data. Mano teaches a register which stores

the comparison data (**Mano**, page 352, figure 7-6(a); EN R0 would store the input data.

R1 is equivalent to 4 in figure 1 of applicant. R2 is equivalent to 14 in figure 1 of

applicant.); and a comparator coupled to the input data node and the register, the

comparator operable to compare the input data with the comparison data. (**Mano**, page

29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input

AND gate; EN 'AND' is only one of many comparison models to use. To construct a

comparator using only AND gates with n inputs, a total of n-1 and gates is needed. Let

the 'X' input be connected to the register and the 'Y' input be connected to the input.). It

would have been obvious to a person having ordinary skill in the art at the time of

applicant's invention to modify teachings of Tseng by having known data stored in a

register and using it to compare with incoming data as taught by Mano to store the

comparison data; and a comparator coupled to the input data node and the register, the

comparator operable to compare the input data with the comparison data.

For the purpose of having a working schematic diagram that fulfills the purpose

of storing data and comparing it with incoming data.

Claim 3.

Tseng, Mano, Barstow Hellstrand and Miller do not teach the bus input of the at

least one look-up table is coupled to a first bus input of the comparator and wherein a

bus output of the register (4), (14) is coupled to a second bus input of the comparator

and also to the register data bus output of the at least one look-up table, and wherein an

output of the comparator is coupled to the result output of the at least one look-up table.

Udagawa teaches the bus input of the at least one look-up table is coupled to a first bus

input of the comparator and wherein a bus output of the register (4), (14) is coupled to a

second bus input of the comparator and also to the register data bus output of the at

least one look-up table, and wherein an output of the comparator is coupled to the result

output of the at least one look-up table (**Udagawa**, figure 4 and C9:47 through C10:8;

EN Udagawa has these three modules set up te same way as applicant.). It would have

been obvious to a person having ordinary skill in the art at the time of applicant's

invention to modify combined teachings of Tseng, Mano, Barstow Hellstrand and Miller

by illustrating the connections between the look-up table, comparator and the register

as taught by Udagawa to illustrate the bus input of the at least one look-up table is

coupled to a first bus input of the comparator and wherein a bus output of the register

(4), (14) is coupled to a second bus input of the comparator and also to the register data

bus output of the at least one look-up table, and wherein an output of the comparator is

coupled to the result output of the at least one look-up table.

For the purpose of having a schematic diagram that illustrates the connections

between the look-up table, comparator and register

Claims 4, 8 and 14.

Tseng does not teach the configurable logic blocks are realized in Field

Programmable Gate Array (FPGA) technology. Mano teaches teach the configurable

logic blocks are realized in Field Programmable Gate Array (FPGA) technology (**Mano,**

pages 330-334). It would have been obvious to a person having ordinary skill in the art

at the time of applicant's invention to modify teachings of Tseng by using logic blocks

that can be programmed as taught by Tseng to have the configurable logic blocks are

realized in Field Programmable Gate Array (FPGA) technology.

For the purpose of short development time, lower production costs, and favorable

system modifications.

Claim 5.

Tseng does not teach the output of the CLB control logic serving as an output of

the CLB. Mano teaches the output of the CLB control logic serving as an output of the

CLB (**Mano**, page 351 figure 7-5(b); EN The contents of this figure are sections (but not

all inclusive) of the CLB and the 2-to-1 MUX, the OR gate with K1 and K2 as inputs for

the OR gate, and R0 comprises the CLB control logic. One can see the 4 inputs K1,

K2, $R2(Q_{0-3})$ and $R1(Q_{0-3})$ result in a single output $R0(Q_{0-3})$). It would have been

obvious to a person having ordinary skill in the art at the time of applicant's invention to

modify teachings of Tseng by designing the schematic so that the final result would be

outputted from the CLB control logic as taught by Mano to have output of the CLB

control logic serving as an output of the CLB.

For the purpose of having a single output in the CLB.

Claim 6.

Mano teaches a register (**Mano**, page 352, figure 7-6(a); EN See claim 2); a

comparator with a first input coupled to the register and with a second input coupled to

an input node (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31

(a)Graphic symbol for a 2 input AND gate; EN See Claim 2, the connection to the

register is the 'X' input and the connection to the input node is the 'Y' input.);

a multiplexer with an input coupled to the register (**Mano**, page 29, table 2-1 (truth table

for 'AND' page 30) page 31 (a)Graphic symbol for a 2 input AND gate; EN See claim 2).

Mano does not teach a control block with inputs coupled to the multiplexer, the

comparator, the input node and an input control node, wherein the logic circuit realizes

an "if then else" branch based upon information carried at the input node and

information stored in the register. Nataraj teaches a control block with inputs coupled to

the multiplexer (**Nataraj**, ¶[0043]), the comparator (**Nataraj**, ¶[0248]), the input node

and an input control node (**Nataraj**, ¶[0155]), wherein the logic circuit realizes an "if

then else" (**Nataraj**, ¶[0094]) branch based upon information carried at the input node

and information stored in the register. It would have been obvious to a person having

ordinary skill in the art at the time of applicant's invention to modify teachings of Mano

by illustrating the relationships us multiplexers, inputs, comparators with CLB for

realizing a if-then-else as taught by Nataraj to a control block with inputs coupled to the

multiplexer, the comparator, the input node and an input control node, wherein the logic

circuit realizes an "if then else" branch based upon information carried at the input node

and information stored in the register.

For the purpose of illustrating the modules needed to have a if-then-else realized.

Claim 7.

Mano teaches the logic circuit comprises a configurable logic block (**Mano**, page 351 figure 7-5(b) See claim 5. Register of applicant is equivalent to R0 of Mano. Comparator of applicant is equivalent to the OR gate of Mano. And the input node of applicant is equivalent to the 4 inputs K1, K2, R1(Q_{0-3}) and R2(Q_{0-3}) of Mano).

Claim 9.

Mano teaches a second register (**Mano**, page 352, figure 7-6(a); EN See claim 2); a second comparator with a first input coupled to the second register and with a second input coupled to the input node (**Mano**, page 352, figure 7-6(a) and page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; EN See claims 2 and 6); a second multiplexer with an input coupled to the second register (**Mano**, page 352, figure 7-6(a); EN See claim 2).

Mano does not teach the control block is coupled to the second comparator and the second multiplexer. Nataraj teaches the control block is coupled to the second comparator and the second multiplexer (**Nataraj**, ¶[0248]). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Mano by having a second pair of comparator and multiplexer so further comparisons can be made as taught by Nataraj to have the control block is coupled to the second comparator and the second multiplexer.

For the purpose of having the expandable capabilities for future uses.

Claim 10.

Mano teaches the output of the CLB control logic serving as an output of the

logic circuit (**Mano**, page 351 figure 7-5(b); EN See claim 5).

Claim 11.

Mano and Nataraj do not teach means for performing a switching function of at

least one conditional branch is implemented with content addressability, wherein the

means for performing a switching function generates an "if then else" branch that

realizes a comparison of input data with previously stored comparison data; means,

coupled to the means for performing a switch function, for selecting at least a portion of

the comparison data; and a CLB control logic circuit having a first input coupled to

receive at least a portion of the input data, a second input coupled to the means for

performing a switching function, and a third input coupled to the means for selecting.

Barstow teaches means for performing a switching function of at least one

conditional branch is implemented with content addressability, wherein the means for

performing a switching function generates an "if then else" branch that realizes a

comparison of input data with previously stored comparison data (**Barstow**, C12:36

through C13:2); means, coupled to the means for performing a switch function, for

selecting at least a portion of the comparison data (**Barstow**, C12:36 through C13:2 and

C14:65 through C15:17; EN ln C12:36 through C13:2 Barstow illustrates the steps taken when going through the 'if' , 'then' and 'else' conditions. In order to make the changes between these steps is called a switch which Barstow illustrates in C14:65 through C15:17.). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Mano and Nataraj by having the ability to switch as needed for an 'if then else' branch as taught by Barstow to have the means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data; means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data.

For the purpose of being able to switch after a select has been chosen.

Mano, Nataraj and Barstow do not teach a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting. Nomura teaches a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting (**Nomura**, C8:9-10 and 45-55). It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings Mano, Nataraj and Barstow by having three inputs related to input data, selecting and

switching as taught by Nomura to have a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

For the purpose of determining what stage the circuit is currently is in to make the next correct move.

Claim 12.

Mano teaches means for storing the comparison data (**Mano**, page 352, figure 7-6(a); EN See claim 2; Comparison data would be stored in R1 or R2.); and means for comparing the comparison data and the input data (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; EN See claim 2).

Claim 13.

Mano teaches a register that stores the comparison data (**Mano**, page 352, figure 7-6(a); EN See claim 2; Comparison data would be stored in R1 or R2.) ; and a comparator coupled to the register and to an input data node that carries the input data (**Mano**, page 29, table 2-1 (truth table for 'AND' page 30) page 31 (a) Graphic symbol for a 2 input AND gate; EN See claim 2).

Conclusion

8.   The prior art of record and not relied upon is considered pertinent to the

applicant's disclosure.

-U. S. Patent 5134693: Saini

-U. S. Patent 6239626: Chesavage

-U. S. Patent Publication 20020157078: Wang

-U. S. Patent Publication 20020113618: Bal

-U. S. Patent Publication 20010037482: Plants

-U. S. Patent 6459303: Chang

-U. S. Patent 6433578: Wasson

-U. S. Patent 6340897: Lytle

-U. S. Patent 6339819: Huppenthal

-U. S. Patent 6034542: Ridgeway

9.   Claims 1-14 are rejected.

Correspondence Information

10.   Any inquiry concerning this information or related to the subject disclosure should

be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-

5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45

p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor David Vincent can be reached at (571) 272-3687. Any response to this

office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

Customer Service Window,

Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 273-8300 (for formal communications intended for entry.)

Information regarding the status of an application may be obtained from the

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unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions

on access to Private PAIR system, contact the Electronic Business Center (EBC) at

866-217-9197 (toll free).

Peter Coughlan

1/4/2006